

IN THE CLAIMS

1. (Original) A method comprising:
fetching coordinate data for a pixel to be rendered;
fetching texel values corresponding to the pixel;
filtering the texel values through a programmable filter; and
outputting a filtered texture value for the pixel.
2. (Original) The method of Claim 1 wherein filtering texel values comprises:
reading a control register; and
using at least one location specified in the control register as a source location.
3. (Original) The method of Claim 1 wherein fetching coordinate data comprises:
retrieving X, Y, Z coordinate data from a vertex pipeline.
4. (Original) The method of Claim 1 further comprising:
writing coordinate fraction data to a plurality of registers.
5. (Original) The method of Claim 1 wherein outputting comprises:
writing the filtered texture value to a register; and
signaling a processor that the filtered texture value is available.
6. (Original) An apparatus comprising:
a fragment processing module;
a programmable texture filtering module in communication with the fragment processing module to programmably filter texture data corresponding to at least one pixel; and
a frame buffer processing module to combine filtered texture data with an existing frame buffer.
7. (Original) The apparatus of Claim 6 wherein the programmable texture filtering module comprises:
a plurality of control registers;
a plurality of source registers;
a plurality of temporary registers; and
at least one output register.

8. (Original) The apparatus of Claim 7 wherein the source registers are read only.

9. (Original) The apparatus of Claim 7 wherein the plurality of control registers comprises:

- a status register;
- an address register;
- an offset register; and
- a plurality of fraction registers.

10. (Original) The apparatus of Claim 7 where the plurality of the control registers comprise:

at least one sampling register have a bit corresponding to each of the source registers to indicate if sampling of a corresponding source register is required.

11. (Original) The apparatus of Claim 6 wherein the programmable texture filtering module comprises:

- a plurality of processing cores to execute an instruction set.

12. (Original) The apparatus of Claim 6 wherein a subset of the plurality of cores are to execute a filtering program on at least one pixel in parallel.

13. (Original) A system comprising:

- a memory,
- a plurality of texture processing cores (TPC) coupled to the memory to programmably filter texture data;
- a fragment processing module to apply the filtered texture data to at least one fragment; and
- a display to display an image created using the at least one fragment.

14. (Original) The system of Claim 13 wherein the plurality of TPC and the fragment processing module are integrated with a host processor.

15. (Original) The system of Claim 13 wherein the plurality of TPCS and the fragment processing module reside in a graphics coprocessor.

16. (Original) The system of Claim 13 comprising:

- a register set associated with each TPC of the plurality.

17. (Original) The system of Claim 15 further comprising:
an accelerated graphics port coupling the graphics coprocessor to the memory.

18. (Original) A computer readable storage media containing executable computer program instructions which when executed cause a digital processing system to perform a method comprising:

fetching coordinate data for a pixel to be rendered;
fetching texel values corresponding to the pixel;
filtering the texel values through a programmable filter; and
outputting a filtered texture value for the pixel.

19. (Original) The computer readable storage media of Claim 18 which when executed cause a digital processing system to perform a method further comprising:

reading a control register; and
using at least one location specified in the control register as a source location.

20. (Original) The computer readable storage media of Claim 18 which when executed cause a digital processing system to perform a method further comprising:

retrieving X, Y, Z coordinate data from a vertex pipeline.

21. (Original) The computer readable storage media of Claim 18 which when executed cause a digital processing system to perform a method further comprising:

writing coordinate fraction data to a plurality of registers.

22. (Original) The computer readable storage media of Claim 18 which when executed cause a digital processing system to perform a method further comprising:

writing the filtered texture value to a register; and
signaling a processor that the filtered texture value is available.

CONCLUSION

The specification is amended to remove any reference to FIG. 1A and FIG. 1B. Applicant respectfully submits that no new matter has been added by Applicant's amendment.

In view of the foregoing, it is believed that all claims now pending are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Thomas Coester

Thomas M. Coester, Reg. No. 39,637

Dated: June 14, 2004

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Missing Parts, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 14, 2004.

Susan Barrette

Susan M. Barrette

6/14/2004

June 14, 2004